Magnetic Digital Isolator
Hermetic Quad Channel

IB8240
IB8241
IB8242

Features

- Hermetic 16-pin SOIC package
- High-speed operation: up to 150Mbps
- No start-up initialization required
- Wide Operating Supply Voltage：2.5V-5.5V
- 60-year life at rated working voltage
- High electromagnetic immunity
- Ultra low power (typical)：
  - 5V Operation, 1.6mA per channel at 1Mbps
  - 5V Operation, 5.5mA per channel at 100Mbps
  - 2.5V Operation, 1.5mA per channel at 1Mbps
  - 2.5V Operation, 3.5mA per channel at 100Mbps
- Enable terminal controls tristate output
- Schmitt trigger inputs
- Transient Immunity 50 kV/μs
- 1000Vdc isolation voltage
- Wide temperature range：–55°C to +125 °C

Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Schematic Diagram

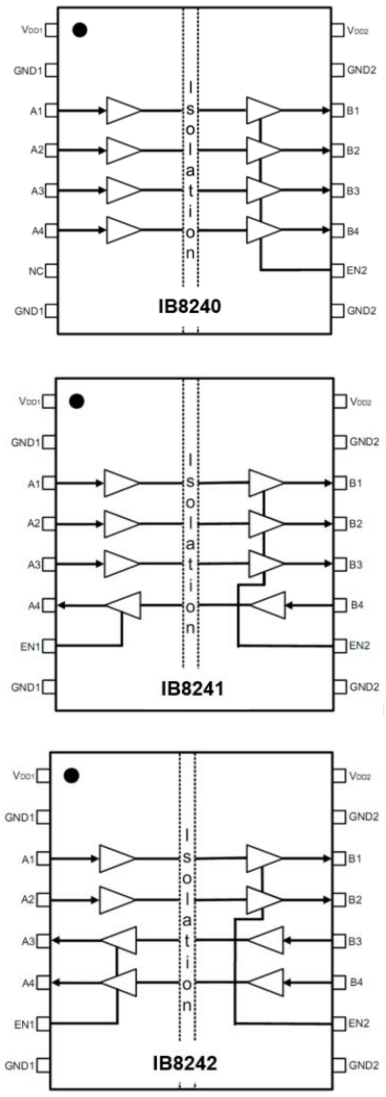

Figure 1. IB824X Schematic Diagram

Absolute Maximum Rating at 25ºC (Note 1)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Storage temperature	T_{STG}	-65	-	150	ºC
Operating temperature	T_A	-55	-	125	ºC
Maximum Junction Temperature	T_J	-	-	150	ºC
Supply Voltage	V_{DD1}, V_{DD2}	-0.50	-	7	V
Input Voltage	V_I	-0.5	-	V_{DD}+0.5	V
Output Voltage	V_O	-0.5	-	V_{DD}+0.5	V
Output Current Drive Channel	I_O	-	-	22	mA
Device Power Dissipation	P_D	-	-	150	mW

Notes

1. When using this product, please observe the absolute maximum ratings. Only one parameter may be set at the limit to ensure no damage to the device. Exceeding any of the limits listed here may damage the device.

ESD Precaution

Please be advised that normal static precautions should be taken in the handling and assembly of this device to prevent damage or degradation which may be induced by electrostatic discharge (ESD).

Recommended Operating Conditions

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Ambient Operating Temperature	T_A	-55	25	125	℃
Supply Voltage	V_{DD}	2.5	-	5.5	V

Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*Min*	*Typ*	*Max*	*Unit*
Vdd Undervoltage Threshold	VDDUV+	VDD1, VDD2 rising	1.95	2.24	2.375	V
Vdd Undervoltage Threshold	VDDUV–	VDD1, VDD2 falling	1.88	2.16	2.325	V
Vdd Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.5	V
High Level Input Voltage	V_{IH}		2.0	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.8	V
High Level Output Voltage	V_{OH}	I_{OH} = – 4 mA	V_{DD1},V_{DD2} –0.4	V_{DD1},V_{DD2} –0.2	-	V
Low Level Output Voltage	V_{OL}	I_{OH} = 4 mA	-	0.2	0.4	V
Input Leakage Current	I_L		-	-	±10	uA
Output Impedance	Z_O		-	50	-	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	-	2.0	-	uA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	-	2.0	-	uA

Timing Characteristics

Maximum Data Rate			0	-	150	Mbps
Minimum Pulse Width			-	-	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 3	-	-	13	ns
Pulse Width Distortion $\lvert t_{PLH} – t_{PHL}\rvert$	PWD	See Figure 3	-	-	4.5	ns
Propagation Delay Skew	$t_{PSK(P-P)}$		-	-	4.5	ns
Channel-Channel Skew	t_{PSK}		-	-	2.5	ns
Output Rise Time	tr	C_L = 15 pF, See Figure 3	-	2.5	4.0	ns
Output Fall Time	tf	C_L = 15 pF, See Figure 3	-	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		-	350	-	ps
Common Mode Transient	CMTI	$V_I = V_{DD}$ or 0 V, V_{CM} = 1500 V, See Figure 4	35	50	-	kV/µs
Enable to Data Valid	t_{en1}	See Figure 2	-	6.0	11	ns
Enable to Data Tristate	t_{en2}	See Figure 2	-	8.0	12	ns
Startup Time	t_{SU}		-	15	40	us

DC Supply Current

- Operating at V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –55 to 125 °C

Parameter	*Symbol*	*Test Condition*	*Min*	*Typ*	*Max*	*Unit*
DC Supply Current (All inputs 0 V or at Supply)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	1.0	1.6	mA
V_{DD2}	I_{DD2}	V_I=0	-	2.4	3.8	mA
V_{DD1}	I_{DD1}	V_I=1	-	6.1	9.2	mA
V_{DD2}	I_{DD2}	V_I=1	-	2.5	4.0	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	1.4	2.2	mA
V_{DD2}	I_{DD2}	V_I=0	-	2.3	3.7	mA
V_{DD1}	I_{DD1}	V_I=1	-	5.2	7.8	mA
V_{DD2}	I_{DD2}	V_I=1	-	3.6	5.4	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	1.8	2.9	mA
V_{DD2}	I_{DD2}	V_I=0	-	1.8	2.9	mA
V_{DD1}	I_{DD1}	V_I=1	-	4.4	6.6	mA
V_{DD2}	I_{DD2}	V_I=1	-	4.4	6.6	mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	2.9	4.0	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	3.4	4.8	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.3	4.6	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	3.3	4.6	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.3	4.6	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	4.0	5.6	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	3.7	5.2	mA
V_{DD2}	I_{DD2}	V_I=0	-	4.1	5.8	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	3.9	5.4	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.9	5.4	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	17.5	22.8	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	7.3	9.8	mA
V_{DD2}	I_{DD2}	V_I=0	-	14.3	18.5	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	11	14.3	mA
V_{DD2}	I_{DD2}	V_I=0	-	11	14.3	mA

- Operating at V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10% , T_A = –55 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Current (All inputs 0 V or at Supply)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	1.0	1.6	mA
V_{DD2}	I_{DD2}	V_I=0	-	2.4	3.8	mA
V_{DD1}	I_{DD1}	V_I=1	-	6.1	9.2	mA
V_{DD2}	I_{DD2}	V_I=1	-	2.5	4.0	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	1.4	2.2	mA
V_{DD2}	I_{DD2}	V_I=0	-	2.3	3.7	mA
V_{DD1}	I_{DD1}	V_I=1	-	5.2	7.8	mA
V_{DD2}	I_{DD2}	V_I=1	-	3.6	5.4	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	1.8	2.9	mA
V_{DD2}	I_{DD2}	V_I=0	-	1.8	2.9	mA
V_{DD1}	I_{DD1}	V_I=1	-	4.4	6.6	mA
V_{DD2}	I_{DD2}	V_I=1	-	4.4	6.6	mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	2.9	4.0	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	3.4	4.8	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.3	4.6	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	3.3	4.6	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.3	4.6	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.4	4.7	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	3.5	4.9	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.6	5.1	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.6	5.0	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	12.3	15.9	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	5.9	7.9	mA
V_{DD2}	I_{DD2}	V_I=0	-	10.3	13.4	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	8.2	10.7	mA
V_{DD2}	I_{DD2}	V_I=0	-	8.2	10.7	mA

- V_{DD1} = 2.5 V±10%, V_{DD2} = 2.5 V±10%, T_A = –55 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Current (All inputs 0 V or at Supply)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	1.0	1.6	mA
V_{DD2}	I_{DD2}	V_I=0	-	2.4	3.8	mA
V_{DD1}	I_{DD1}	V_I=1	-	6.1	9.2	mA
V_{DD2}	I_{DD2}	V_I=1	-	2.5	4.0	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	1.4	2.2	mA
V_{DD2}	I_{DD2}	V_I=0	-	2.3	3.7	mA
V_{DD1}	I_{DD1}	V_I=1	-	5.2	7.8	mA
V_{DD2}	I_{DD2}	V_I=1	-	3.6	5.4	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	1.8	2.9	mA
V_{DD2}	I_{DD2}	V_I=0	-	1.8	2.9	mA
V_{DD1}	I_{DD1}	V_I=1	-	4.4	6.6	mA
V_{DD2}	I_{DD2}	V_I=1	-	4.4	6.6	mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	2.9	4.0	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	3.4	4.8	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.3	4.6	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	3.3	4.6	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.3	4.6	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.1	4.3	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	3.5	4.8	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.4	4.8	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	3.4	4.8	mA
V_{DD2}	I_{DD2}	V_I=0	-	3.4	4.8	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
IB8240						
V_{DD1}	I_{DD1}	V_I=0	-	3.6	5.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	9.9	12.8	mA
IB8241						
V_{DD1}	I_{DD1}	V_I=0	-	5.2	7.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	8.5	11.1	mA
IB8242						
V_{DD1}	I_{DD1}	V_I=0	-	6.9	9.0	mA
V_{DD2}	I_{DD2}	V_I=0	-	6.9	9.0	mA

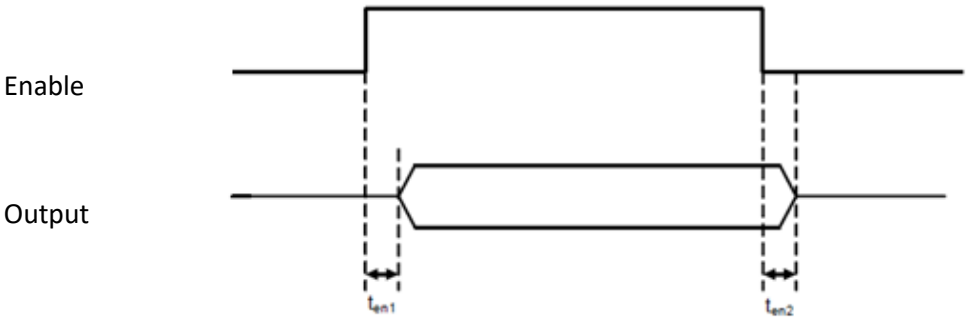

Figure 2. Enable Delay Timing

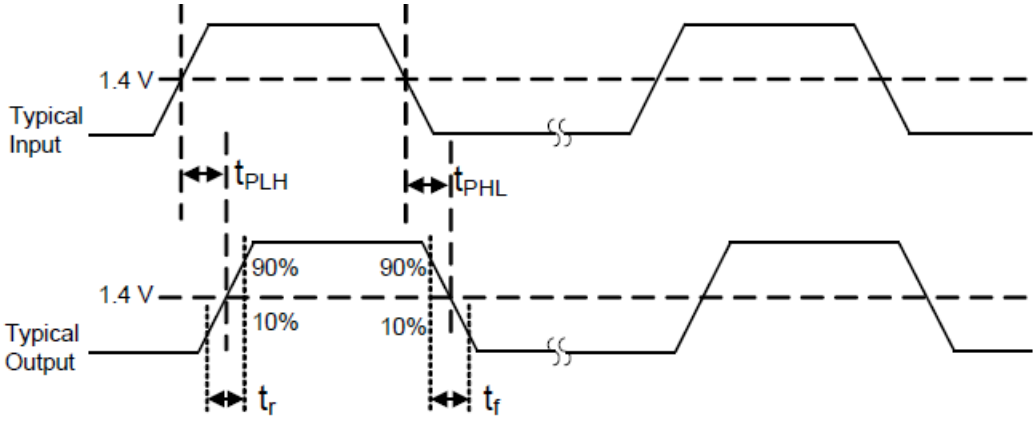

Figure 3. Propagation Delay Timing

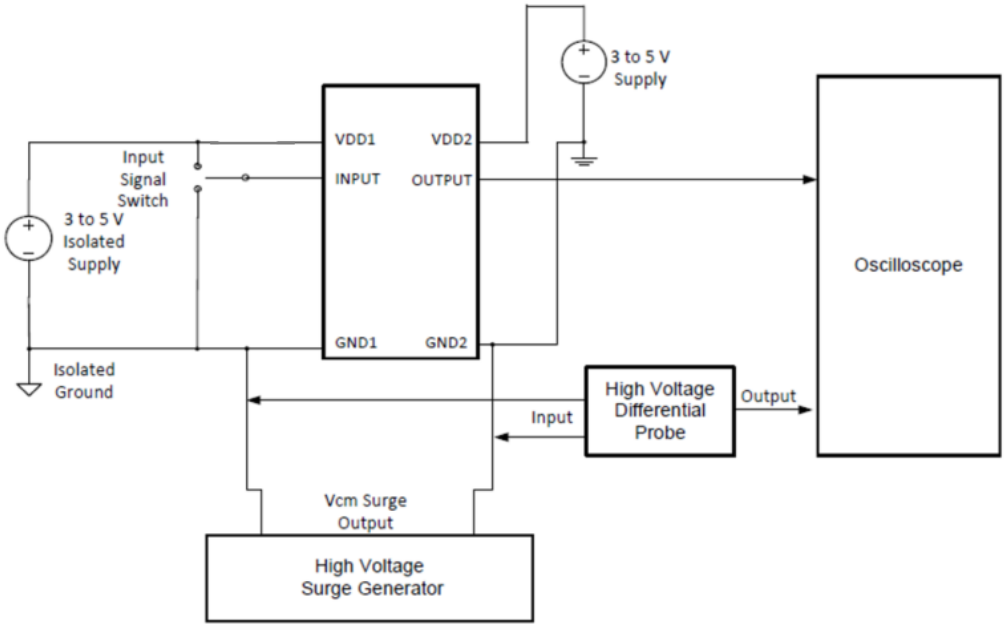

Figure 4. Common Mode Transient Immunity Test Circuit

Logic Operation

V_I Input	*EN Input*	*VDDI State*	*VDDO State*	*VO Output*	*Description*
H	H or NC	P	P	H	Normal operation
L	H or NC	P	P	L	Normal operation
X[3]	L	P	P	Hi-Z	Forbidden
X[3]	H or NC	UP	P	L	
X[3]	L	UP	P	Hi-Z	Forbidden
X[3]	X[3]	P	UP	Uncertain	

Notes :

1. VDDI and VDDO are the input and output power supplies. VI and VO are the respective input and output terminals.
2. X= Not Applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance
3. "Powered" state (P) is defined as 2.5 V < VDD < 5.5 V.
4. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
5. NC replaces EN1 in some devices. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
6. UP=Unpowered, defined as VDD=0.
7. When using the enable pin (EN) function, the output pin state is driven into a high-impedance state when the EN pin is disabled (EN = 0).

Truth Table

P/N	*EN1*	*EN2*	*Description*
IB8240	-	H	Output B1, B2, B3, B4 are enabled and follow the input state
	-	L	Output B1, B2, B3, B4 are disabled and in high impedance state
IB8241	H	X	Output B1, B2, B3, B4 are enabled and follow the input state
	L	X	Output A4 are disabled and in high impedance state
	X	H	Output B1, B2, B3 are enabled and follow the input state
	X	L	Output B1, B2, B3 are disabled and in high impedance state
IB8242	H	X	Output A3, A4 are enabled and follow the input state
	L	X	Output A3, A4 are disabled and in high impedance state
	X	H	Output B1, B2 are enabled and follow the input state
	X	L	Output B1, B2 are disabled and in high impedance state

Undervoltage Lockout :

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when VDD1 falls below VDD1(UVLO–) and exits UVLO when VDD1 rises above VDD1(UVLO+). Side B operates the same as Side A with respect to its VDD2 supply.

Reference proposal :

The IB8240 family requires a 0.1 µF bypass capacitor between VDD1 and GND1 and VDD2 and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300Ω) in series with the inputs and outputs if the system is excessively noisy.

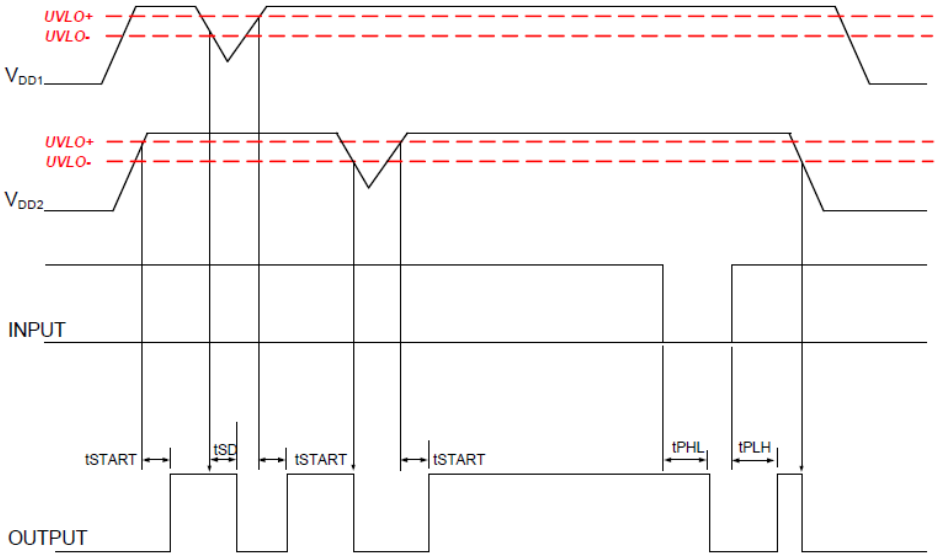

Figure 5. Device Behavior during Normal Operation

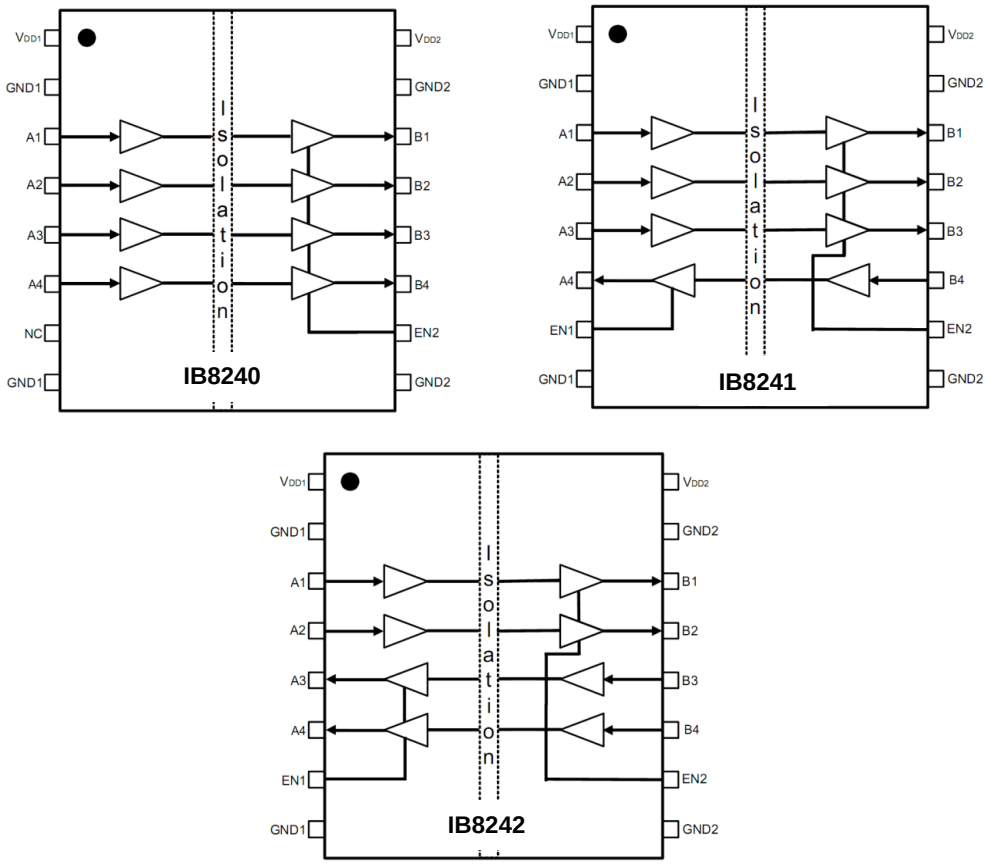

Figure 6. IB824X Connection Diagrams

Pin Configuration

Name	*Pin #*	*Type*	*Description*
VDD1	1	Supply	Side 1 Power Supply
GND1	2	Ground	Side 1 Ground
A1	3	Digital Input	Side 1 Digital Input
A2	4	Digital Input	Side 1 Digital Input
A3	5	Digital I/O	Side 1 Digital Input or Output
A4	6	Digital I/O	Side 1 Digital Input or Output
EN1/NC	7	Digital Input	Side 1 High Level enable input
GND1	8	Ground	Side 1 Ground
GND2	9	Ground	Side 2 Ground
EN2	10	Digital Input	Side 2 High Level Enable Input
B4	11	Digital I/O	Side 2 Digital Input or Output
B3	12	Digital I/O	Side 2 Digital Input or Output
B2	13	Digital Output	Side 2 Output
B1	14	Digital Output	Side 2 Output
GND2	15	Ground	Side 2 Ground
VDD2	16	Supply	Side 2 Supply

Package Dimensions in inches (mm)

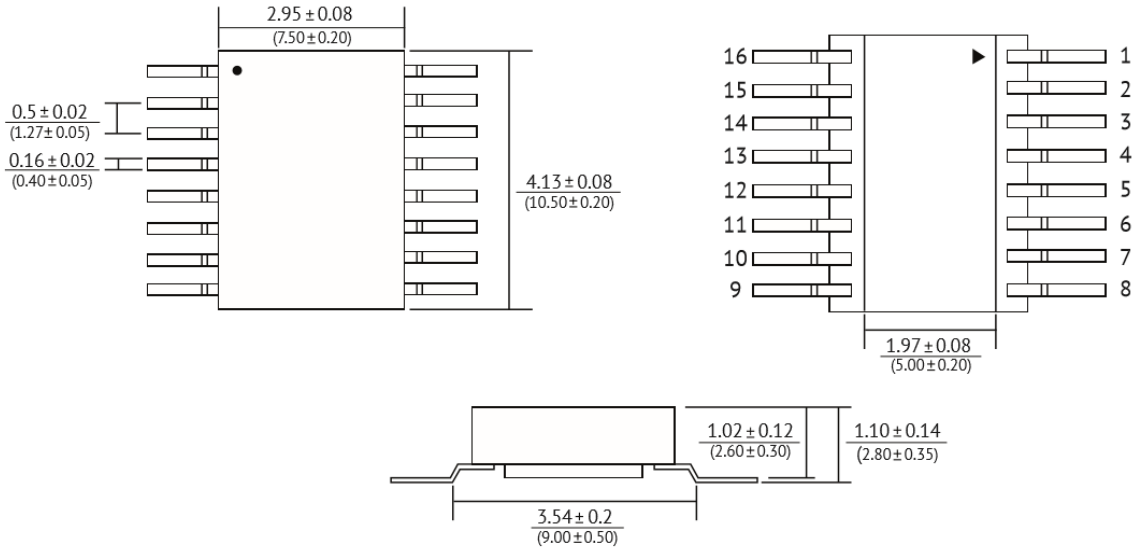

Figure 7. IB824X Package Dimensions

Ordering Information

Manufacturing Part Number	*Part Description*
IB8240	Hermetic Magnetic Digital Isolator Quad Channel 16-pin SOIC Package
IB8241	Hermetic Magnetic Digital Isolator Quad Channel 16-pin SOIC Package
IB8242	Hermetic Magnetic Digital Isolator Quad Channel 16-pin SOIC Package

DISCLAIMER